REMARKS

I. Status of claims

Applicants have amended claim 1-21 to improve clarity and to more appropriately define the invention. Applicants have also added new claims 22-27 to protect additional aspect of the present invention. Upon entry of this Amendment, claims 1-27 are pending and under current examination.

II. Regarding the Office Action

In the Office Action of July 27, 2005, the Examiner objected to the specification for informalities; objected to claims 5 and 15 for informalities; rejected claims 8-14 under 35 U.S.C. § 101 for being directed to non-statutory subject matter; rejected claims 2, 6, 9, 16, and 20 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement; rejected claims 5, 8-14, and 19 under 35 U.S.C. § 112, second paragraph, for being indefinite; and rejected claims 1-21 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,484,297 to *Dixit et al.* ("*Dixit*"). Applicants address the objections and rejections below.

III. Objection to the informalities in the specification and the claims

Applicants have amended the specification, on page 13 and page 19, to correct typographical and grammatical errors. Applicants have also amended claims 5 and 15 to correct the typographical errors pointed out by the Examiner.

In response to the Examiner's objection to the use of term "dispersion" in the claims, Applicants have amended the claims to instead recite the term "variation." Although "variation" is not used explicitly in the specification, dispersion and variation are interchangeable in the context of the present application. Generally, when data

values for a particular feature or parameter are not all the same, the variation among such values can be called dispersion. In the specification, for example, on page 7, lines 17-31, the term dispersion generally refers to variation of data values, such as voltage level of a signal, width of a polysilicon, thickness of an oxide film, etc. Applicants therefore submit that amending the claims to recite "variation" overcomes the Examiner's objection.

As such, Applicants have corrected the informalities in the specification and the claims by this Amendment. Accordingly, the objections to informalities should be withdrawn.

IV. Rejection of claims 8-14 under 35 U.S.C. § 101

Applicants have amended claims 8-14 to recite "a computer-executed logical simulation method." The amended claims 8-14 are directed to new and useful processes, and are therefore directed to statutory subject matter. Accordingly, the rejection of claims 8-14 under 35 U.S.C. § 101 should be withdrawn.

V. Rejection of claims 2, 6, 9, 16, and 20 under 35 U.S.C. § 112

In the Office Action, the Examiner rejected claims 2, 6, 9, 16, and 20 under 35 U.S.C. § 112, first paragraph. The Examiner pointed out that, in the claims, "[the method or a component] corrects said design information on the basis of said dispersion" is not supported in the specification (OA at 4). Applicants have amended these claims, and respectfully submit that these amended claims are supported by the specification.

For example, beginning at page 11, line 31, when describing Figure 2, the specification states that "[i]f the result of the simulation is not coincident with the

expected value (step S9), the design net list F2 is modified (step S10), and the above described series of steps are repeated (steps S2 through S9). Specifically, the modification of the design net list F2 is carried out by the modification of the circuit layout and the revision of the power supply method, and by a redesign if the detected operational malfunction is significant."

As such, claims 2, 6, 9, 16, and 20 are supported by the specification to convey to one skilled in the art, that Applicants had possession of the claimed invention at the time the application was filed. Accordingly, the rejection of these claims under 35 U.S.C. § 112 should be withdrawn.

Claims 5, 12, and 19 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite. The Examiner pointed out that "verifying whether abnormality is caused in the transmission of the said signal by the difference in said power supply voltage in the same chip" is not clearly described in the specification (OA, at 5).

Applicants have amended these claims to clarify antecedent support in the claim language and to improve clarity. The amended claims are clearly supported by the specification. For example, in describing a third preferred embodiment on page 13, the specification describes power supply voltages being different in respective cells of the same chip (Page 13, lines 5 - 31). Further, when the power supply voltage on the signal transmitting side AN2c is different from the power supply voltage on the signal receiving side AN2d, "operational problems might be caused in an actual circuit, so that there is some possibility that the transmission of signals is not normally carried out" (Page 14, lines 11-15). The specification further explains that in such cases, a logical simulation part 10 of a logical simulation system 1, shown in FIG. 1, has the function of receiving

information of a dispersion rule file F4 via a delay information operating part 12 to carry out a rule check on the basis of this information (Page 14, lines 15-20).

Claims 8-14 were also rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicants have amended the claims to ensure proper antecedent basis for the elements recited in the claims.

As such, Applicants respectfully submit that the claims 5, 8-14, and 19, as amended, particularly point out and distinctly claim the subject matter. Accordingly, the rejections under 35 U.S.C. § 112, second paragraph, should be withdrawn.

VI. Regarding claims interpretation

Each amended clear is clear on its face. Applicants do not subscribe to the Examiner's interpretation of claims as stated in the Office Action (OA, at 6). Applicants respectfully submit that the amended claims particularly point out and distinctly claim the subject matter, and should be examined as such.

VII. Rejection of claims 1-21 under 35 U.S.C. § 102(e)

Applicants traverse the rejection of claims 1-21 under 35 U.S.C. § 102(e) because *Dixit* does not teach each and every element of these claims. In order to properly anticipate Applicants' claimed invention under 35 U.S.C. § 102(e), each and every element of the claim in issue must be found, either expressly described or under principles of inherency, in a single prior art reference. Further, " [t]he identical invention must be shown in as complete detail as is contained in the...claim." See M.P.E.P. § 2131 (8th Ed., Aug. 2001), quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Finally, "[t]he elements must be arranged as required by the claim." M.P.E.P. § 2131 (8th Ed. 2001), p. 2100-69.

Dixit discloses methods for calculating delays for cells in ASICs (Abstract). In *Dixit*, delays are computed by considering not only the process (P), voltage (V), temperature (T) but also input ramptime (R) and output load or fanout (F) of the cells by fitting the delay at four corner points for derated PVT condition into a non-linear equation which is a function of P, V, T, R and F (Abstract). *Dixit* further discloses that the delay is a five-dimensional (P, V, T, R and F) characterization (Abstract). In *Dixit*, delays are computed by considering not only the process (P), voltage (V), temperature (T) but also input ramptime (R) and output load or fanout (F) of the cells (Col. 4, line 66 - Col. 5, line 6). Further, *Dixit* discloses that given R and F, the values for Kp, Kt and Kv can be solved by using the discussed equations (Col. 7, lines 45-46). Further, after solving for Kp, Kt and Kv, those values are applied to another equation to solve for any new delays for the cells (Col. 7, lines 47-59).

However, *Dixit* does not teach a delay information operating part further receiving design information of an integrated circuit to prepare a delay information file incorporating each influence of variation of electrical and physical characteristics for each location in a chip on the basis of a variation rule file and design information, as required by claim 1.

Thus, *Dixit* fails to teach each and every element of claim 1. Therefore *Dixit* cannot anticipate claim 1 under 35 U.S.C. 102(e). Accordingly, Applicants request the withdrawal of the rejection of claim 1, and claims 2-7 which depend from claim 1, and the allowance of claims 1-7.

Independent claims 8 and 15, although of different scope, recite features similar to those of claim 1. Therefore, for at least the reasons *Dixit* does not anticipate claim 1,

Dixit also does not anticipate claims 8 and 15. Accordingly, Applicants request the withdrawal of the rejection of claims 8 and 15, and claims 9-14 and 16-21 which depend from claims 8 and 15, respectively, and the allowance of claims 8-21.

Further, new claims 22-27 are also patentable over *Dixit* at least due to their dependence from one of the independent claims 1, 8, and 15.

VIII. Conclusion

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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